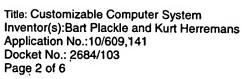
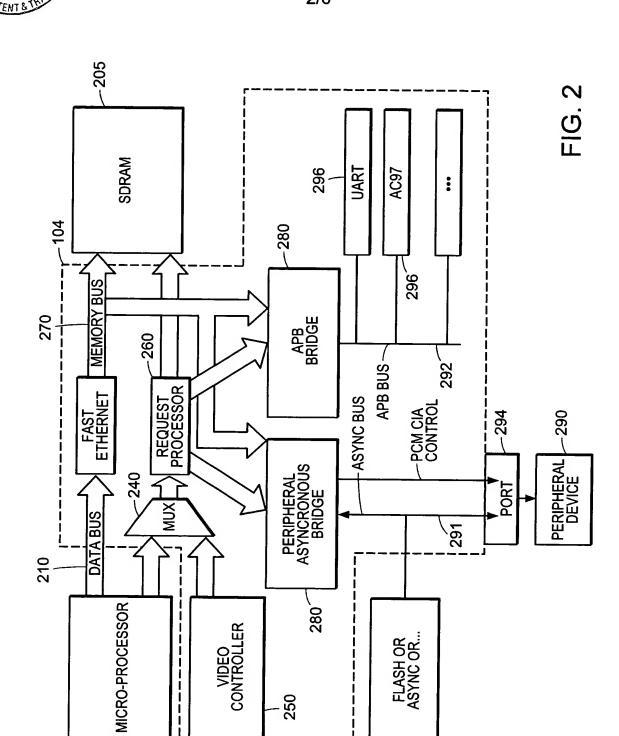
Title: Customizable Computer System Inventor(s):Bart Plackle and Kurt Herremans Application No.:10/609,141 Docket No.: 2684/103 Page 1 of 6 1/6 160 PROCESSOR INDEPENDENT HARDWARE **IEEE 1384** CUSTOM **J1850 CA11 AC97 1**2C INTERRUPT CONTROLLER 160 PERIPHERAL DEVICE FAST ETHERNET **PCMCIA** CPIO USB SPI 160 130 BRIDGE 150 MEMORY CONTROLLER 185 **V**0 PROCESSOR DEPENDENT HARDWARE 190 EXTERNAL BUS INTERFACE 180 PROPRIETARY INTERFACE 104 103 EXTERNAL BUS INTERFACE MICRO-PROCESSOR PROCESSOR CORE I & D CACHE 102



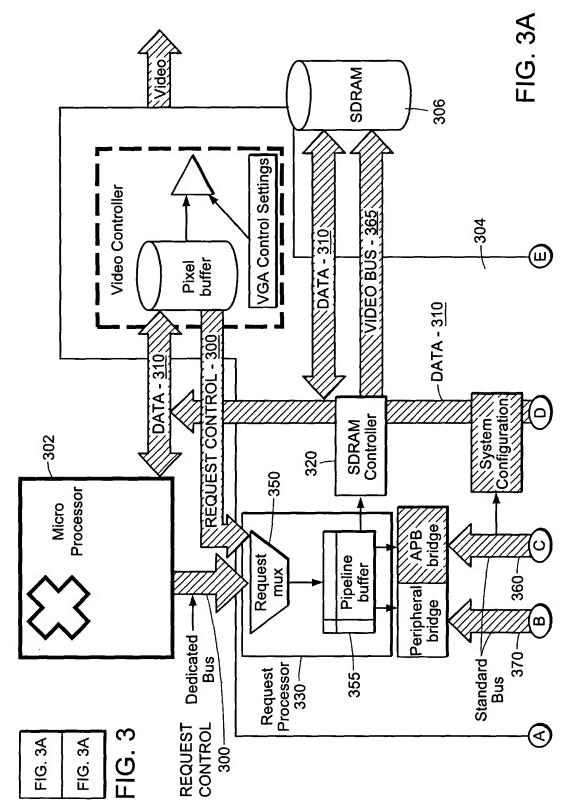
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Title: Customizable Computer System Inventor(s):Bart Plackle and Kurt Herremans Application No.:10/609,141 Docket No.: 2684/103 Page 3 of 6



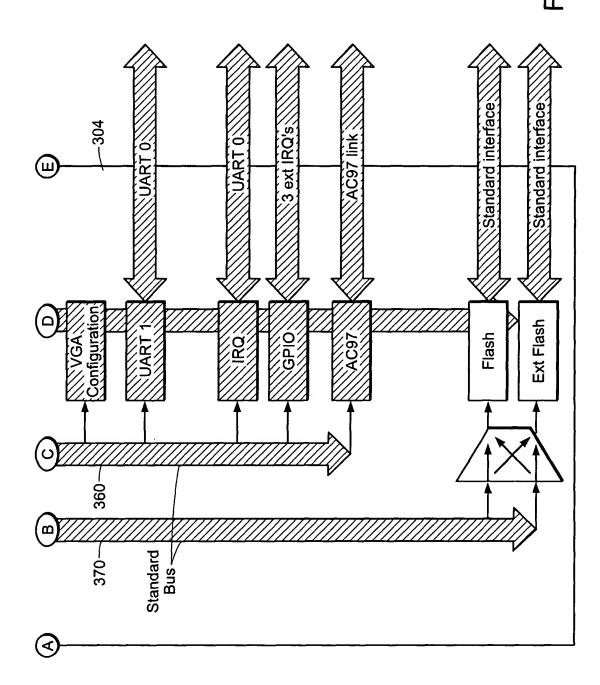
3/6



Title: Customizable Computer System Inventor(s):Bart Plackle and Kurt Herremans Application No.:10/609,141 Docket No.: 2684/103 Page 4 of 6



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Title: Customizable Computer System Inventor(s):Bart Plackle and Kurt Herremans Application No.:10/609,141 Docket No.: 2684/103 AUG O B 2003 Page 5 of 6 5/6 -185 Video Controller 452 32 bit address Pos 1 R/W #B|P|a|S|A[28:00] Pos 0 R/W #B|p|a|s A[28:00] (ပ command 120 Muxed Address Pos 2 Pos 3 · Issue1 Cycle1 · Issue1 Cycle0 Issue2 Cycle1 Issue2 Cycle0 103 Pos 1 |R/W #B|P|a|S|A[28:16]|A[15:00] p|A|s|A[28:16]|A[15:00] Demuxed 32 bit address Processor Issue Bus Muxed Command Demuxed command Pos 0 R/W #B Pos 3 Pos 2 lssue FIFO dependant (translation process bus to < internal FIFO) (Top layer of bridge) Highly processor 130 FIG. 4 FIG. 4A FIG. 4A

